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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,084	01/03/2002	Robert J. Falster	MEMC 98-3052 (2512.2)	7363

321 7590 01/28/2004

SENNIGER POWERS LEAVITT AND ROEDEL
ONE METROPOLITAN SQUARE
16TH FLOOR
ST LOUIS, MO 63102

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,084	FALSTER, ROBERT J.	
	Examin r	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Status of the Claims

1. Amendment filed November 7, 2003 has been entered. Claims 1-46 have been canceled. Claims 47 and 51 have been amended. Claims 52 has been added, thus, claims 47-52 are pending.

Terminal Disclaimer

2. The terminal disclaimer filed on November 7, 2003 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 6,236,104 and 6,342,725 have been reviewed and is accepted. The terminal disclaimer has been recorded.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 47, 48 and 52 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 3 and 11 of U.S. Patent No. 5,919,302 in view of Nakato et al. (U.S. Patent No. 5,436,175) (of record).

Patent '302 teaches a single crystal silicon device layer comprising a central axis, a circumferential edge, a radius extending from the central axis to the circumferential edge and a first axially symmetric region which is vacancy dominated and substantially free of agglomerated vacancy-type defects. wherein the first axially symmetric region comprises the central axis of the device layer and has a width as measured in the radial direction from the central axis towards the circumferential edge which is at least about 15 mm.

Thus, patent '302, claimed substantially all limitation of the current claim with the exception being used in an SOI structure.

However Nakato teaches: a high quality wafer can be used in an SOI structure including:

a single crystal silicon device layer (12);

a single crystal handle wafer (14); and

an insulating oxide layer (26) between the device layer (12) and the handle wafer (14).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use the device layer of patent '302 in the formation of the SOI structure as taught by Nakato to avoid junction leakage since the device layer is defect free.

With respect to "the width of at least about 15mm", this width encompasses 7.5% of the radius.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 47-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakato et al. (U.S. Patent No. 5,436,175) in view of Park et al (U.S. Patent No. 6,045,610) (all of record).

Nakato teaches a silicon on insulator (SOI) structure substantially similar as claimed including:

a single crystal silicon device layer (12);

a single crystal silicon handle wafer (14); and,

an insulating oxide layer (26) between the device layer and the handle wafer.

Thus Nakato is shown to teach all the features of the claim with the exception of explicitly disclosing the characteristics of the single crystal silicon device layer (12).

However, Park teaches forming a semiconductor wafer from CZ ingot having (V/G) ratio control including: a central axis, a circumferential edge, a radius extending from the central axis to the circumferential edge and a first axially symmetric region (V) which is vacancy dominated and substantially free of agglomerated vacancy-type defects, wherein the first axially symmetric region (V) comprises the central axis (A) of the device laver and has a width

as measured in the radial direction from the central axis (A) towards the circumferential edge which is at least about 7.5% of the radius of the device layer. (See Figs. 3D, 4D, 11 and 12, col. 3, line 63-col. 4, line 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the SOI structure of Nakato using semiconductor substrate as taught by Park to avoid junction leakage characteristics caused by well known dislocation clusters (agglomerated vacancy-type defects).

Although Park does not explicitly disclosing "the axially symmetric region (V) has a width as measured in the radial direction from the central axis (A) towards the circumferential edge which is at least about 7.5% of the radius of the device layer", however, Park discloses that: the pure region (P) is at least 36% of the wafer area. More preferably, the pure region is at least 60% of the wafer area" (col. 6, ll. 1-5). From these value one having ordinary skill in the art should easily obtain a value that includes "at least 7.5% of the radius of the device layer".

With respect to claim 48, the wafer of Park is grown by CZ method thus, inherently has an oxygen content less than about 13 PPMA.

With respect to claim 49, the handle wafer (14) of Nakato, in view of Park, further comprises two major, generally parallel surfaces, one of which is the front surface and the other of which is the back surface of the silicon wafer (14), a central plane between the front and back surfaces, the circumferential edge joining the front and back surfaces, a surface layer which comprises a first region of the silicon wafer between the front surface and a distance, D1, of at

least about 10 micrometers, as measured from the front and a bulk layer which surface and toward the central plane, comprises a second region of the silicon wafer between the central plane and the first region, the silicon wafer having a non-uniform concentration of vacancies with the concentration of vacancies in the bulk layer being greater than the concentration of vacancies in the surface layer such that, upon subjecting the wafer to an oxygen precipitation heat treatment, a denuded zone is formed in the surface layer and oxygen clusters or precipitates are formed in the bulk layer with the concentration of the oxygen clusters or precipitates in the bulk layer being primarily dependant upon the concentration of vacancies.

These are the inherent characteristics of the SOI substrate under thermal anneal following the implantation.

With respect to claim 50, the handle wafer (14) of Nakato, in view of Park, further comprises two major, generally parallel surfaces, one of which is the front surface and the other of which is the back surface of the silicon wafer (14), a central plane between the front and back surfaces, the circumferential edge joining the front and back surfaces, and a denuded zone which comprises the region of the silicon wafer from the front surface to a distance, D1, of at least about 10 micrometers, as measured in the direction of the central plane, and which contains interstitial oxygen, the silicon wafer having a concentration of interstitial oxygen in the denuded zone at a distance equal to about one-half of D, is at least about 75% of the maximum concentration of interstitial oxygen in the denuded zone.

These are the inherent characteristics of the SOI substrate under thermal anneal following the implantation.

With respect to claim 51, the handle wafer (14) of Nakato, in view of Park, further comprises two major, generally parallel surfaces, one of which is the front surface and the other of which is the back surface of the silicon wafer (14), a central plane between the front and back surfaces, the circumferential edge joining the front and back surfaces, a front surface layer consisting of a first region of the silicon wafer within a distance, D, of no more than about 15 micrometers from the front surface and a bulk layer comprising a second region of the silicon wafer between the central plane and the front surface layer, the bulk layer having a substantially uniform oxygen concentration and a concentration of crystal lattice vacancies.

These are the inherent characteristics of the SOI substrate under thermal anneal following the implantation.

Product by process limitation:

The expression "*such that upon subjecting the silicon wafer to an oxygen precipitation heat treatment consisting essentially of annealing the silicon wafer at 800 °C for four hours and then at 1000 °C for sixteen hours, the silicon wafer will contain oxygen precipitates having a concentration profile in which the peak density of the precipitates in the bulk layer is at or near the central plane with the concentration of the precipitates in the bulk layer generally decreasing in the direction of the front surface layer*" is taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it

is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

With respect to the dimension of 10 and 15 micrometers of claims 49-51, note that the specification contains no disclosure of either the *critical nature of the claimed dimension of any unexpected results arising therefrom*. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

With respect to claim 52, as shown in Figs. 11 and 12, by choosing a proper location of a wafer within an ingot, one having ordinary skill in the art should easily obtain a wafer which results in the axially symmetric region (V) has a width which is at least about 15% of the radius of the device layer. Furthermore, the similar reasoning as that of claim 47 also encompass the claimed "15%".

Response to Arguments

5. Applicant's arguments with respect to claims 47-51 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
January 16, 2004

LONG PHAM
PRIMARY EXAMINER